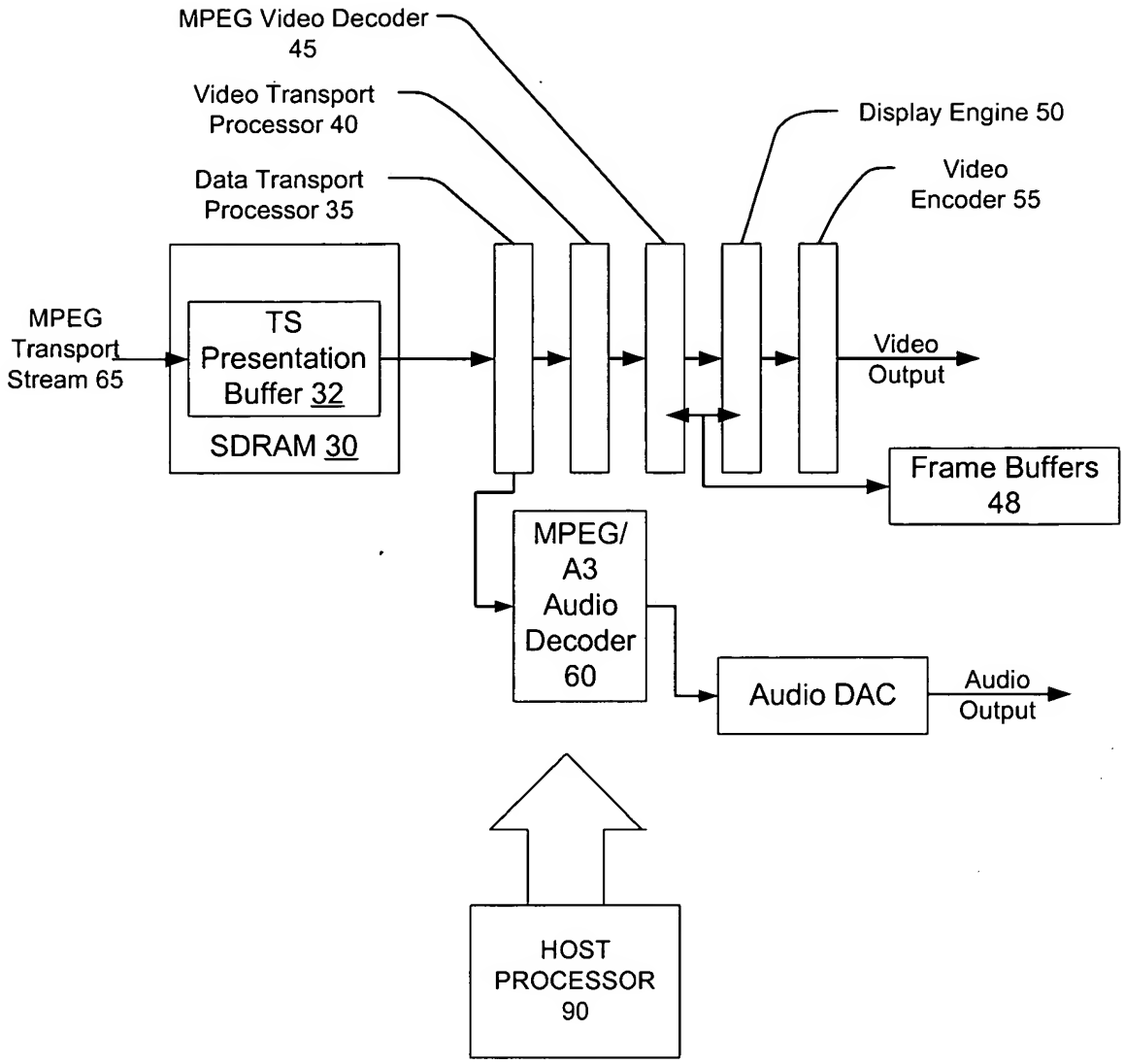

MPEG Video Decoder 45
Video Transport Processor 40
Data Transport Processor 35
Display Engine 50
Video Encoder 55
MPEG Transport Stream 65
TS Presentation Buffer 32
SDRAM 30
Video Output
Frame Buffers 48
MPEG/ A3 Audio Decoder 60
Audio DAC
Audio Output
HOST PROCESSOR 90

FIG. 1

100(0)	YC	Y	YC	Y	.....	YC	Y	YCr	Y	YCr	Y	YCr	Y
100(1)	YC	Y	YC	Y	.....	YC	Y	YCr	Y	YCr	Y	YCr	Y
100(2)	YC	Y	YC	Y	.....	YC	Y	YCb	Y	YCb	Y	YCb	Y
100(3)	YC	Y	YC	Y	.....	YC	Y	YCb	Y	YCb	Y	YCb	Y
100(4)	YC	Y	YC	Y	.....	YC	Y	YCr	Y	YCr	Y	YCr	Y
100(5)	YC	Y	YC	Y	.....	YC	Y	YCr	Y	YCr	Y	YCr	Y
100(6)	YC	Y	YC	Y	.....	YC	Y	YCb	Y	YCb	Y	YCb	Y
:													
:													
100(N)	YC	Y	YC	Y	.....	YC	Y	YCb	Y	YCb	Y	YCb	Y

FIGURE 2

FIGURE 4

Top Field	100(0)	YC	Y	YC	Y	.....	YC Y
	100(2)	YC	Y	YC	Y	.....	YC Y
	100(4)	YC	Y	YC	Y	.....	YC Y
	100(6)	YC	Y	YC	Y	.....	YC Y
	:						
	100(N-1)	YC	Y	YC	Y	.....	YC Y
Bottom Field	100(1)	YC	Y	YC	Y	.....	YC Y
	100(3)	YC	Y	YC	Y	.....	YC Y
	100(5)	YC	Y	YC	Y	.....	YC Y
	100(7)	YC	Y	YC	Y	.....	YC Y
	:						
	100(N)	YC	Y	YC	Y	.....	YC Y

FIGURE 3

100(0) 100(2) : 100(30)	$M_{0,0}^{y}/M_{0,0}^{c}$	$M_{0,1}^{y}/M_{0,1}^{c}$	.....	$M_{0,NMBX-1}^{y}/M_{0,NMBX-1}^{c}$
100(32) 100(34) : 100(62)	$M_{1,0}^{y}/M_{1,0}^{c}$	$M_{1,1}^{y}/M_{1,1}^{c}$	.....	$M_{1,NMBX-1}^{y}/M_{1,NMBX-1}^{c}$
:				
	$M_{NMBY-1,0}^{y}$ $M_{1,0}^{c}$	$M_{NMBY-1,1}^{y}$ $M_{1,1}^{c}$	.....	$M_{NMBY-1,NMBX-1}^{y}$ $M_{1,NMBX-1}^{c}$

Top Field

100(1) 100(3) : 100(31)	$M_{0,0}^{y}/M_{0,0}^{c}$	$M_{0,1}^{y}/M_{0,1}^{c}$	.....	$M_{0,NMBX-1}^{y}/M_{0,NMBX-1}^{c}$
100(33) 100(35) : 100(63)	$M_{1,0}^{y}/M_{1,0}^{c}$	$M_{1,1}^{y}/M_{1,1}^{c}$	.....	$M_{1,NMBX-1}^{y}/M_{1,NMBX-1}^{c}$
:				
	$M_{NMBY-1,0}^{y}$ $M_{1,0}^{c}$	$M_{NMBY-1,1}^{y}$ $M_{1,1}^{c}$	.....	$M_{NMBY-1,NMBX-1}^{y}$ $M_{1,NMBX-1}^{c}$

Bottom Field

FIGURE 5A

TOP FIELD

48Y(0)	YYYYYYYYYYYYYYYY
48Y(1)	YYYYYYYYYYYYYYYY
48Y(2)	YYYYYYYYYYYYYYYY
:	
48Y(15)	YYYYYYYYYYYYYYYY
48Y(16-31)	$M_{0,1}^{y}$
48Y(32-47)	$M_{0,2}^{y}$
:	
	$M_{NMBY-1,NMBX-1}^{y}$
:	
BOTTOM FIELD	
	$M_{0,0}^{y}$
	$M_{0,1}^{y}$
	:
	$M_{0,NMBX-1}^{y}$
	$M_{1,0}^{y}$
	:
	$M_{1,NMBX-1}^{y}$
	:

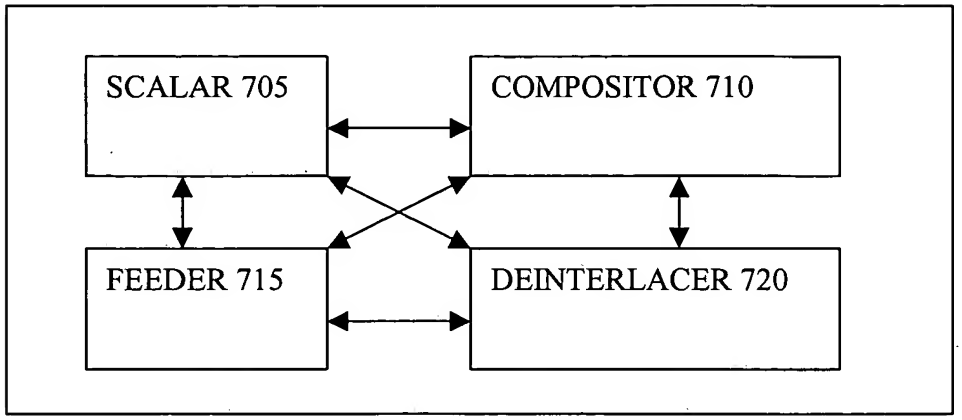
FIGURE 5B

TOP FIELD

48C(0) CbCbCrCrCbCbCrCrCbCbCrCrCbCbCrCr
48C(1) CbCbCrCrCbCbCrCrCbCbCrCrCbCbCrCr
48C(2) CbCbCrCrCbCbCrCrCbCbCrCrCbCbCrCr
:
48C(7) CbCbCrCrCbCbCrCrCbCbCrCrCbCbCrCr
48C(8-15) $\mathbf{M_{0,1}^{c}}$
48C(16-23) $\mathbf{M_{0,2}^{c}}$
:
$\mathbf{M_{NMBC-1,NMBX-1}^{c}}$
:
BOTTOM FIELD
$\mathbf{M_{0,0}^{c}}$
$\mathbf{M_{0,1}^{c}}$
:
$\mathbf{M_{0,NMBX-1}^{c}}$
$\mathbf{M_{1,0}^{c}}$
:
$\mathbf{M_{1,NMBX-1}^{c}}$
:

FIGURE 5C

FIG. 6



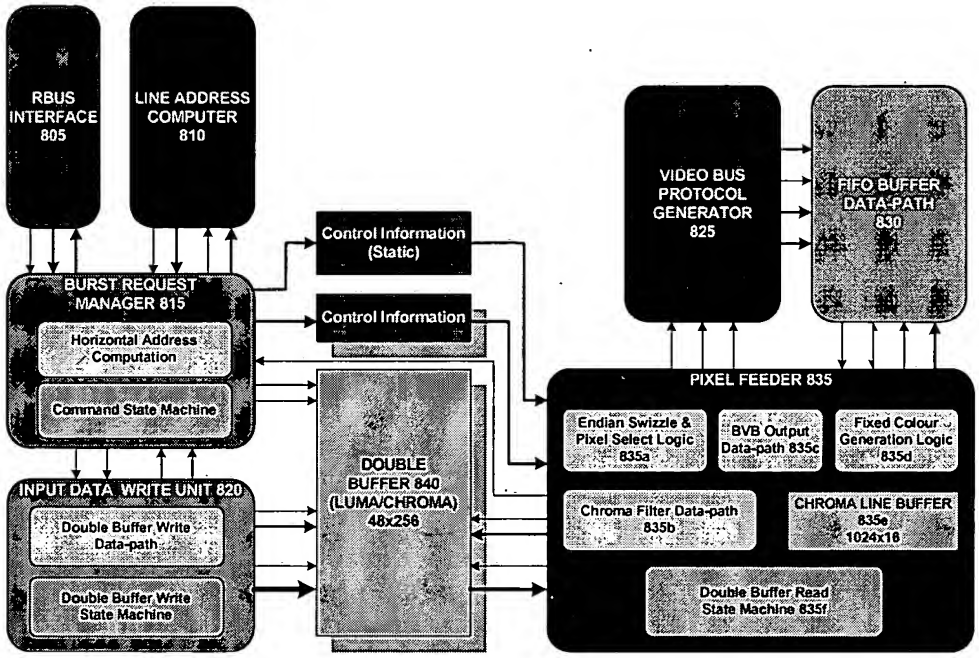


FIGURE 7

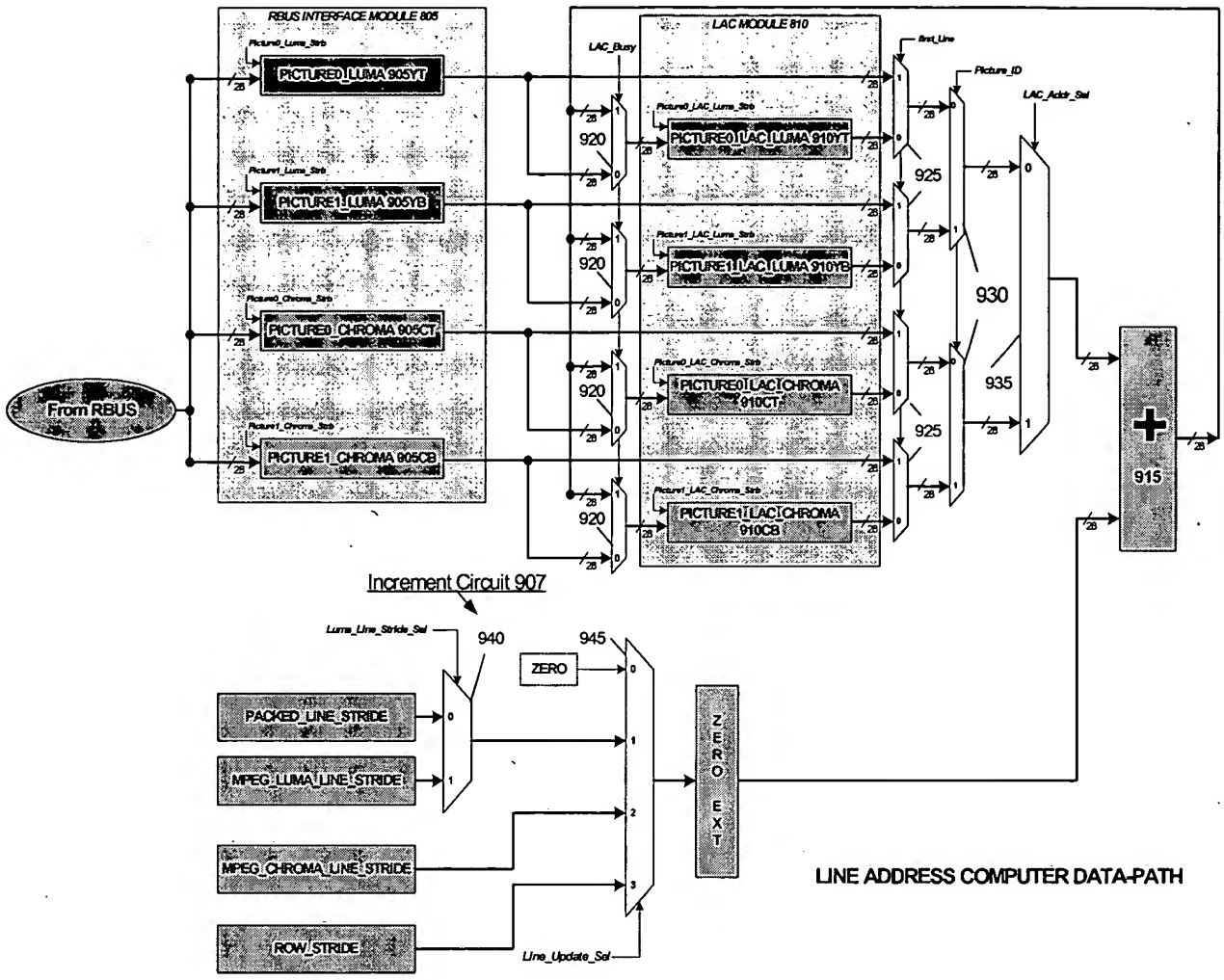

RBUS INTERFACE MODULE 805
LAC MODULE 810
LAC_Busy
PICTURE0_LUMA 905YT
PICTURE1_LUMA 905YB
PICTURE0_CHROMA 905CT
PICTURE1_CHROMA 905CB
From RBUS
PICTURE0_LAC_LUMA 910YT
PICTURE1_LAC_LUMA 910YB
PICTURE0_LAC_CHROMA 910CT
PICTURE1_LAC_CHROMA 910CB
920
925
930
935
915
Increment Circuit 907
940
945
ZERO
PACKED_LINE_STRIDE
MPEG_LUMA_LINE_STRIDE
MPEG_CHROMA_LINE_STRIDE
ROW_STRIDE
ZERO EXT
LINE ADDRESS COMPUTER DATA-PATH

FIGURE 8

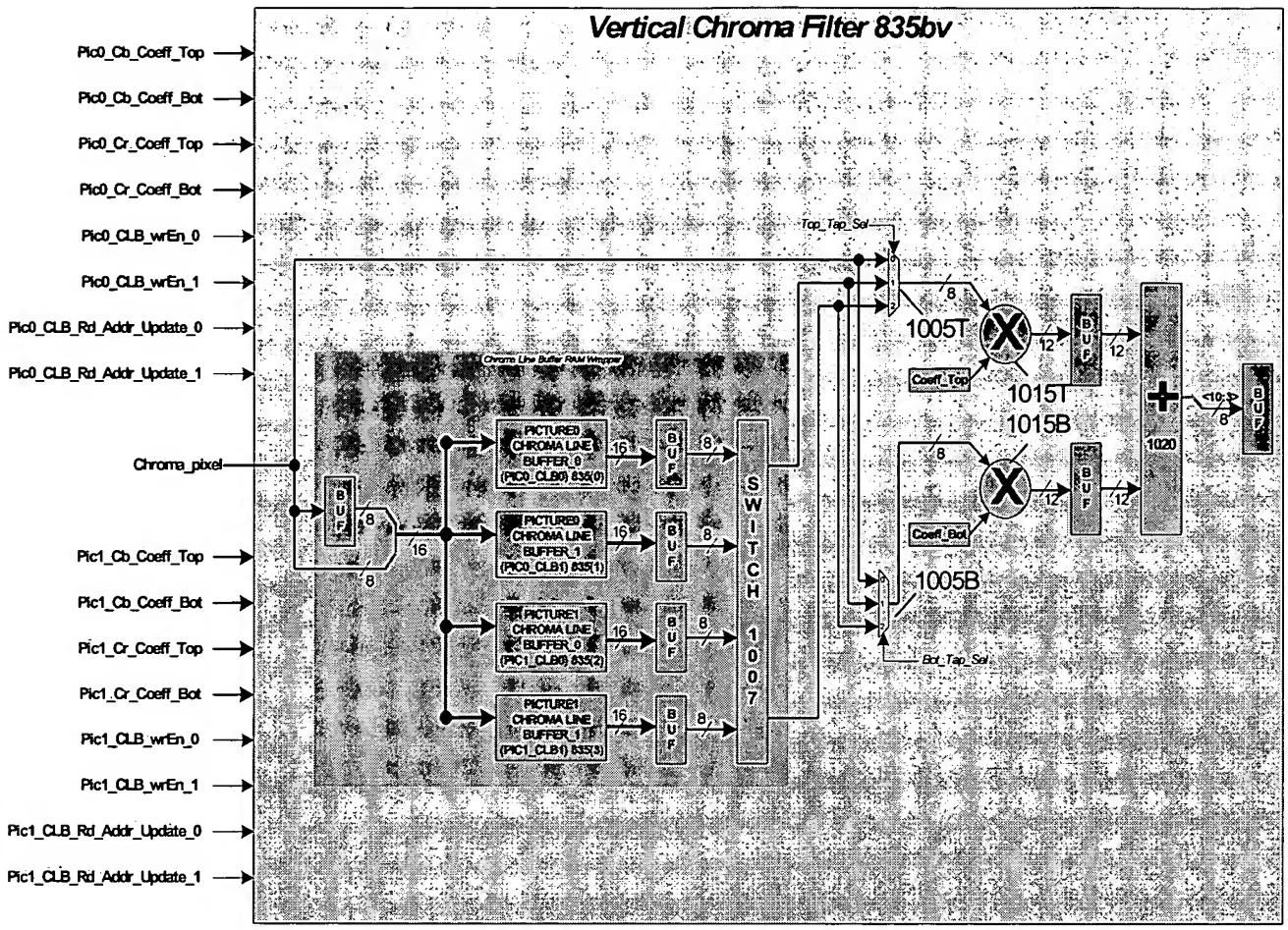

Vertical Chroma Filter 835bv
Pic0_Cb_Coeff_Top
Pic0_Cb_Coeff_Bot
Pic0_Cr_Coeff_Top
Pic0_Cr_Coeff_Bot
Pic0_CLB_wrEn_0
Pic0_CLB_wrEn_1
Pic0_CLB_Rd_Addr_Update_0
Pic0_CLB_Rd_Addr_Update_1
Chroma_pixel
Pic1_Cb_Coeff_Top
Pic1_Cb_Coeff_Bot
Pic1_Cr_Coeff_Top
Pic1_Cr_Coeff_Bot
Pic1_CLB_wrEn_0
Pic1_CLB_wrEn_1
Pic1_CLB_Rd_Addr_Update_0
Pic1_CLB_Rd_Addr_Update_1
Chroma Line Buffer RAM Wrapper
PICTURE0 CHROMA LINE BUFFER_0 (PIC0_CLB0) 835(0)
PICTURE0 CHROMA LINE BUFFER_1 (PIC0_CLB1) 835(1)
PICTURE1 CHROMA LINE BUFFER_0 (PIC1_CLB0) 835(2)
PICTURE1 CHROMA LINE BUFFER_1 (PIC1_CLB1) 835(3)
BUF
SWITCH 1007
Top_Tap_Sel
Bot_Tap_Sel
1005T
1015T
1005B
1015B
Coeff_Top
Coeff_Bot
1020
<10:3>
8
12
16

FIGURE 9